USERGUIDE

UG020 | EDLC Module Calculator, Constant Power Discharge

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1. DESIGN-IN OF CAPACITOR MODULE

The voltage of an electric double-layer capacitor (EDLC) depends on its charging state. Thus, the voltage at the terminals increases or decreases as soon as the EDLC becomes charged or discharged. To provide a stable voltage, the EDLC is often operated with a DC/DC conversion. Depending on the required power and charging voltage V, it is required to design a module as shown in Figure 1.

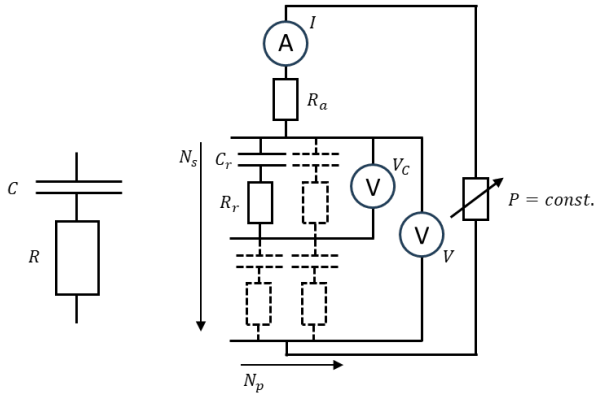


Figure 1: Schematic of EDLC module

The EDLC module must provide the power required by the application. The EDLC Module Calculator calculates the size of the stack (module) based on the application parameter. Based on a given

- power demand,
- discharge time, and
- lower discharge limit,

the calculator provides the number of series and parallel connected EDLCs (defined by rated capacitance C_r and rated Equivalent series resistance (ESR) R_{ESR}) as well as plots and other electrical parameters, such as total module capacitance C and total ESR R.

2. INPUT

At least four values have to be entered in the input section, as shown in Figure 2.

Input								
Input	Cut-off el. stat. volt., module [V]	Charging volt., module [V]	Total power output [W]	Discharge time, [sec]	Manually, increase ESR [Ohm]	Manually, increase series con. [#]	Manually, increase paral. con. [#]	Manually, increase cap. value, C [%]
	3.00	8.00	30.00	16.30				
	Min:2.0785V							

Figure 2: The input section of the module calculator

In the mandatory input field **"Cut-off electrostatic voltage, module"** the lower voltage level (or cut-off) of the EDLC module is entered. It constitutes the electrostatic voltage level of the capacitor after the discharge. As an orientation, this level has to be well above the cut-off of the DC/DC converter, below which the converter will not

work. There is also a lower physical voltage based on the discharge power P and the ESR R below, which a discharge is not possible. It is calculated by $\sqrt{4 \times P \times R}$" " and given below the input field as "Min." The minimum value is calculated from the ESR values of the selected capacitors and may, therefore, not meet the expected cut-off. In such cases, the cut-off needs to be increased, the power output decreased, the series connection increased, or the capacitance increased. This field is mandatory for the calculation. It will be highlighted in red if it is too low.

In the mandatory input field **"Charging voltage, module"** the upper electrostatic charging voltage of the entire capacitor unit is entered. The Charging voltage is often given by the charging limit or upper voltage limit of DC/DC converter or supercapacitor charger. This field is mandatory for the calculation since its input is used to calculate the number of series-connected single-cell EDLCs.

In the mandatory input field **"Total power output"** the constant power (in units of watt) required by the application is entered (this includes inefficiencies of the DC/DC converter as well). The larger the power, the larger the remaining voltage, below which the capacitor cannot be discharged (given in the Field below the Cut-Off voltage). The discharge current causes a voltage drop over the ESR, which prohibits a complete discharge of the capacitor. This field is mandatory for the calculation.

In the mandatory input field **"Discharge time"** the desired time (in units of sec) of operation over which the power should be applied is entered. This field is mandatory for the calculation since its input is used to calculate the capacitive size, including the parallelization of the module.

In the optional filed **"Increase ESR manually"** an additional ESR value R_a (in units of Ohm), which is added to the preselected datasheet ESR value of the EDLC, can be entered. An increase in the ESR may be required due to additional contact resistances or to account for an aging effect, which leads to an increased effective ESR. This field is optional for the calculation and is left blank if unnecessary.

In the optional filed **"Manually, increase parallel. connections"** a number can be entered by which the "Caps, Number in Parallel", which is given in the calculated output, is increased. An increase in parallel capacitors leads to an increase in the module's capacitance. This field is optional for the calculation and is left blank if unnecessary.

In the optional filed **"Manually change capacitance value"** the "Total C, as calculated " value can be changed by any percentage. Such changes might be desirable to account for aging, for instance. This field is optional for the calculation and is left blank if unnecessary.

3. OUTPUT: MINIMALLY REQUIRED, INTERMEDIATE RESULTS

The output field, depicted in Figure 3, shows the minimally required capacitance (Total C [F], as calculated), the series-connected single-cell capacitance (Single cell C [F], as calculated), and the maximally allowed ESR (Max. allowed ESR). Those parameters cannot necessarily be achieved by building a module from commercially available capacitors. The next fitting values for commercially available EDLCs are given in the output: Result (for product). The corresponding discharge behaviour is shown in the blue graphs in the figures.

Output	Min. requ., Intermediate result		
	Total C, as calculated [F]	Single cell C, as calculated [F]	Max. allowed ESR [Ohm]
	18.12254	54.36762	0.075

Figure 3: Output field

The output field **"Total C [F], as calculated"** shows the calculation of the total capacitance C based on the given input. The underlying model assumes the power and energy conservation of the capacitor

$$\underbrace{VI}_{\substack{\text{Power delivered by capacitive unit and corresponds to electrostic stored Energy}}} + \underbrace{RI^2}_{\substack{\text{Power lossed due to current, Power is transfered to heat}}} + \underbrace{P}_{\substack{\text{Power required by the application, usable power, output power}}} = 0$$

with $V(t)$ the electrostatic voltage of the capacitor, $I(t)$ the discharge current, R the equivalent series resistance (ESR) and P the usable output power of the R-C capacitor unit. With the definition of the capacitor current $I = C\frac{dV}{dt}$, were C is the capacitance of the capacitor, the above equation can be solved, leading to

$$C = \frac{t_1 4P}{V_0^2 - V_1^2 + V_0\sqrt{V_0^2 - 4RP} - V_1\sqrt{V_1^2 - 4RP} - 4PR\ln\left(\frac{V_0 + \sqrt{V_0^2 - 4RP}}{V_1 + \sqrt{V_1^2 - 4RP}}\right)}$$

which gives the minimal required capacitance for a certain power output, with t_1 as discharge time, V_1 as the electrostatic lower voltage (Cut-off) level and V_0 as the charging voltage.[1] The value for power output P, charging voltage V_0, cut-off V_1 and discharge time t_1 is entered in the input, while the ESR is determined by using $\frac{V_1^2}{4P} = R_{max} = R$. The values of V_1, P and R have to fulfill the maximum output limit $\frac{V_1^2}{4P} = R_{max} > R$ and are, in that respect, not entirely independent of each other.

The output field **"Single-cell C [F], as calculated"** provides the capacitance of the single cell, as calculated with $C_{cell} = n_s C$, with n_s as the number of series connected capacitors, required to meet the single cell rated voltage limit of 2.7V.

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4. OUTPUT: RESULT (FOR PRODUCT)

The results in the output field, depicted in Figure 4, are based on products from the Würth Elektronik's portfolio. All necessary electrical details are given to implement the EDLC module with single-cell products of Würth Elektronik. The corresponding discharge behavior is shown in the green graphs in the figures.

	Result (for product)										
Output	Single cell, voltage [V]	Single cell, EDLC product, C [F]	Single cell, EDLC product, PN	Total module cap. [F]	Total module ESR [Ohm]	Cap. in parallel [#]	Cap. in series [#]	Total number, Cap. [#]	El. stat. volt. at end of disch. [V]	El. dyn. volt. at end of disch. [V]	Current at end of disch. [A]
	2.67	100	851617031001	33.33	0.036000	1	3	3	5.900	5.672	5.289

Figure 4: Output Field

The output field **"Single cell, voltage"** shows the single-cell voltage of the individual cell. The single-cell voltage limit has to be smaller than the rated voltage V_r, given in the datasheet. The single-cell voltage V_c calculated by the number of serial-connected capacitors N_s with $V_c = \frac{V}{N_s}$.

The output field **"Single cell, EDLC product, C"** shows the single-cell capacitance of the capacitor product C_r, i.e. rated capacitance. It is the next largest available capacitor, compared to the value given in "Single Cell C [F], as calculated" C, hence, $C_r = \left\lceil C \frac{N_s}{N_p} \right\rceil_{PN}$ and $C_r \frac{N_p}{N_s} \geq C$". "

The output field **"Single cell, EDLC product, PN"** gives the corresponding part number (PN) of the single-cell EDLC with C_r. With this selection, the single-cell capacitance, i.e. rated capacitance, C_r and the rated ESR R_r is set for the calculation.

The output field **"Total stack capacitance, C"** shows the total capacitance of the entire module, consisting of the capacitor with capacitance given in "Single Cell, EDLC Product, C [F]". $C = C_r \frac{N_p}{N_s}$.

The output field **"Total ESR"** gives the ESR of the entire capacitor module $R = R_r \frac{N_s}{N_p} + R_a$, which is based on the corresponding datasheet value, including the value given in "Manually, Increase ESR [Ohm]" R_a.

The output field **"Capacitors in parallel"** gives the number of parallel connected capacitors N_p if the value is >1, parallelization of cells is required. The required capacitance cannot be reached by the largest available capacitor (product) in the portfolio, so parallelization is required.

The output field **"Capacitors in series"** gives the number of series connected capacitors $N_s = \left\lceil \frac{V_0}{V_r} \right\rceil$. If the value is >1, a series connection of cells is required.

The output field **"Total number, Capacitors"** gives the total number of capacitors $N_s \times N_p$, required for the module.

The output field **"Electrostatic voltage at end of discharge"** gives the remaining electrostatic voltage of the capacitor
$V_1 = V(t_1)$ after the constant power discharge process.

The output field **"Electrodynamic voltage at end of discharge"** gives the remaining electrodynamic voltage of the capacitor $V_{RC}(t_1) = V(t_1) - R|I(t_1)| = \frac{P}{|I(t_1)|}$ after the constant power discharge process.

The output field **"Current at end of discharge"** gives the discharge current magnitude at the end of discharge $|I(t_1)| = \frac{V(t_1) - \sqrt{V^2(t_1) - 4RP}}{2R}$, i.e. maximum discharge current. It should always be below the current limits of the individual cells and or the entire unit.

5. OUTPUT: GRAPHS

The Figure 5 shows the plot of the discharge current vs. time for the minimal required capacitance (as calculated) as well as for the capacitance of the capacitor unit (for product), implemented with single cells, calculated with $I(t) = \frac{V(t)-\sqrt{V^2(t)-4RP}}{2R}$. The rated current, the maximum current as well as the current at the end of discharge for the entire unit are also given. The current at the end of discharge crosses the discharge curve at the designated discharge time, which is given in the input section. The rated discharge and maximum discharge current, is by definition, the constant current I, necessary to discharge an EDLC from V_0 to $\frac{V_0}{2}$ within Δ t=5 sec and Δ t=1 sec, respectively, as calculated with $I = \frac{\Delta V}{\left(\frac{1}{C}\Delta t + R_{ESR}\right)}$.

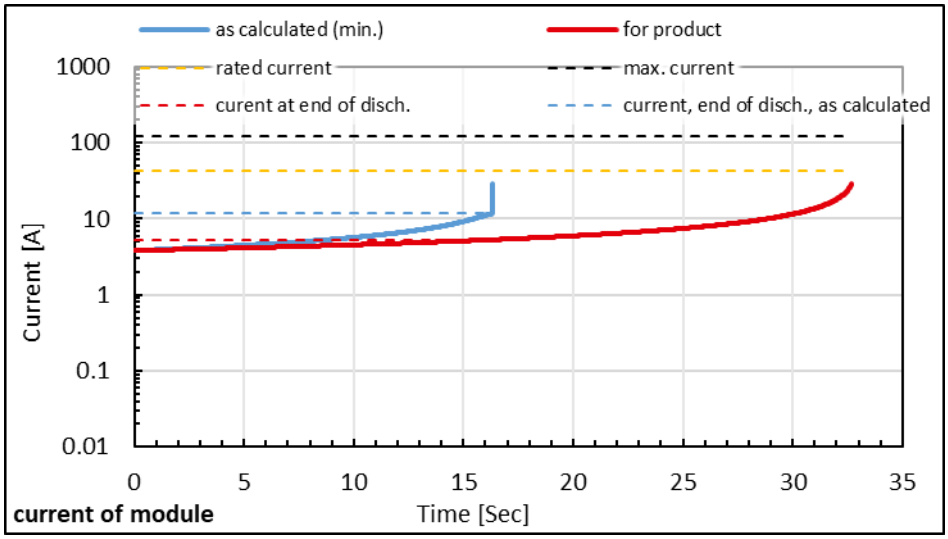


Figure 5: The current of the capacitor module

Figure 6 shows the electrostatic voltage of the capacitor vs. time $V(t)$ for the minimal required capacitance (as calculated) and for the capacitance of the capacitor unit (for product), implemented with single cells. It also shows the cut-off voltage given in the input section and the electrostatic voltage at the end of discharge.

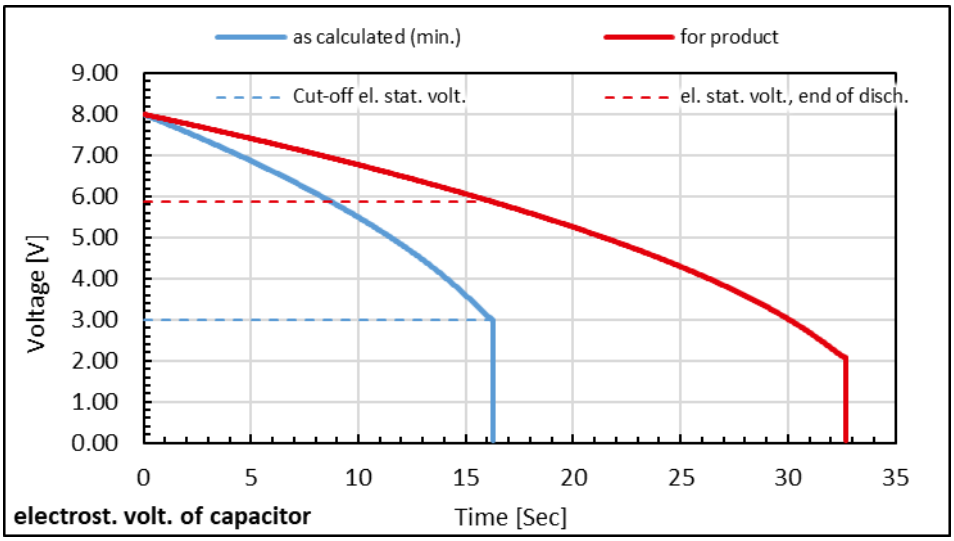


Figure 6: Electrostatic voltage of the capacitor module

Figure 7 shows the electrodynamic voltage of the capacitor vs. time for the minimal required capacitance (as calculated) and for the capacitance of the capacitor unit (for product), implemented with single cells. Voltage includes the voltage drop over ESR as calculated with $V(t) - R|I(t)| = \frac{P}{|I(t)|} = V_{RC}(t)$. It also shows the cut-off voltage given in the input section and the electrodynamic voltage at the end of discharge.

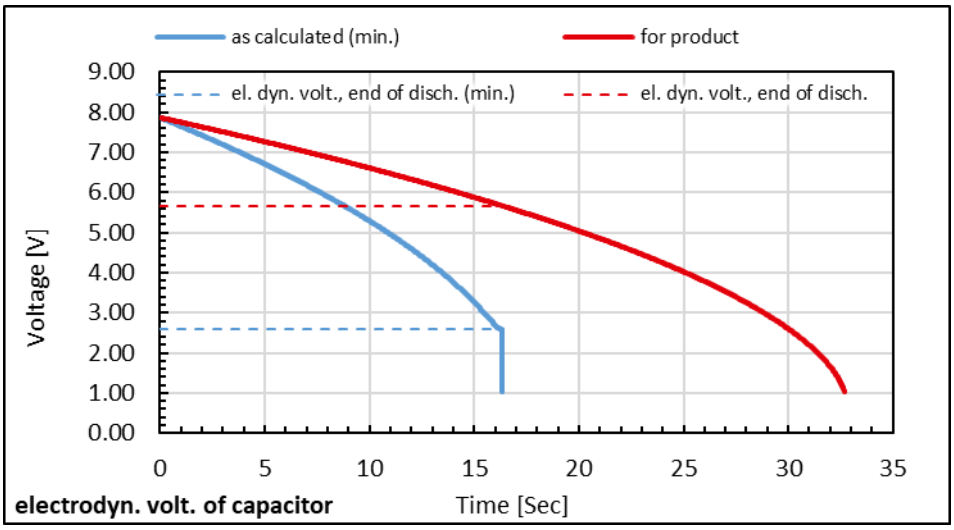


Figure 7: Electrodynamic voltage of the capacitor unit

Figure 8 shows the losses and usable power vs. time for the minimal required capacitance (as calculated) as well as for the capacitance of the capacitor unit (for product), implemented with single cells. The theoretically possible total power output as well as the loss at the end of discharge, are also given. The power at the end of discharge crosses the loss curve at the designated discharge time, which is given in the input section. The losses, i.e. joules heating, increase as the capacitor voltage decreases to keep the power output constant.

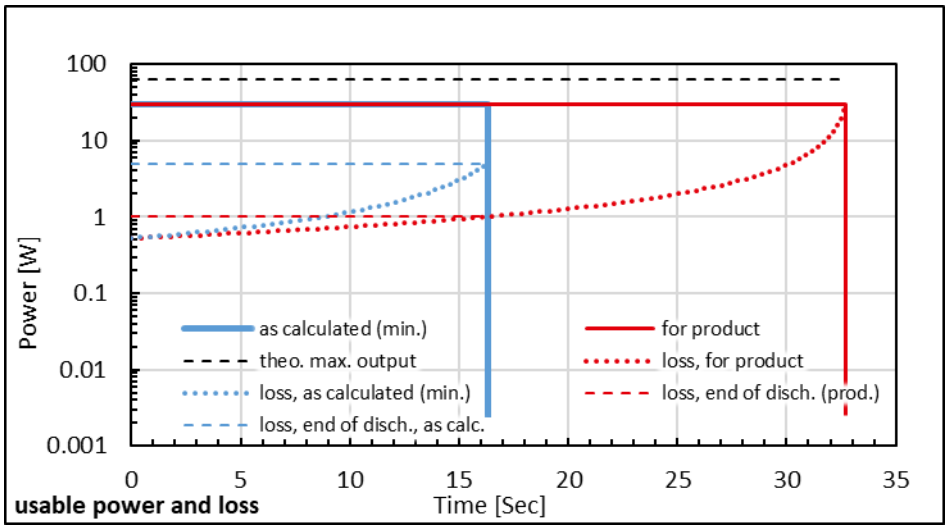


Figure 8: Useable power output and loss of the capacitor module

6. MEASUREMENT EXAMPLE

Measurements presented in Figure 9, Figure 10 and Figure 11 have been made with the Chroma Charge/Discharge Tester C17216M-10-6 for which two test channels have been paralyzed and connected via a test fixture to the EDLC stack. Two different stacks with three series connected 50 F and 100 F have been measured under constant power output to demonstrate the correctness of the Module Calculator's result.

- The calculation parameters
- Cut-off el. stat. volt., module: 3 V,
- Charging volt., module: 8 V,
- Total power output: 30 W and
- Discharge time: 16.2 sec

have been specifically chosen for demonstrational purposes; the measurement of the 50 F stack and the 100 F stack can be described by the "as calculated" graph and the "for product" graph, respectively. Usually, a capacitor stack that matches the discharge characteristic of the "as calculated" graph may not be built from commercially available capacitor sizes. The results from the Output: Result (for product) sections must be used for the implementation.

shows the effect of the ESR, which leads to a voltage drop during the discharge. After the discharge, as shown in the figure's inset, the measured voltage shows a step and returns to the calculated electrostatic voltage. The minor discrepancies here arise from the difference between the actual ESR and the datasheet values. There is also a long-term voltage increase related to internal charge distribution, which shall only be mentioned for the sake of completeness and not further discussed.[2] The voltage step at the end of discharge is more pronounced in the measurement of the 50°F stack. Here, the cell voltage is lower compared to a 100 F stack, requiring larger currents and thus causing a larger voltage step.

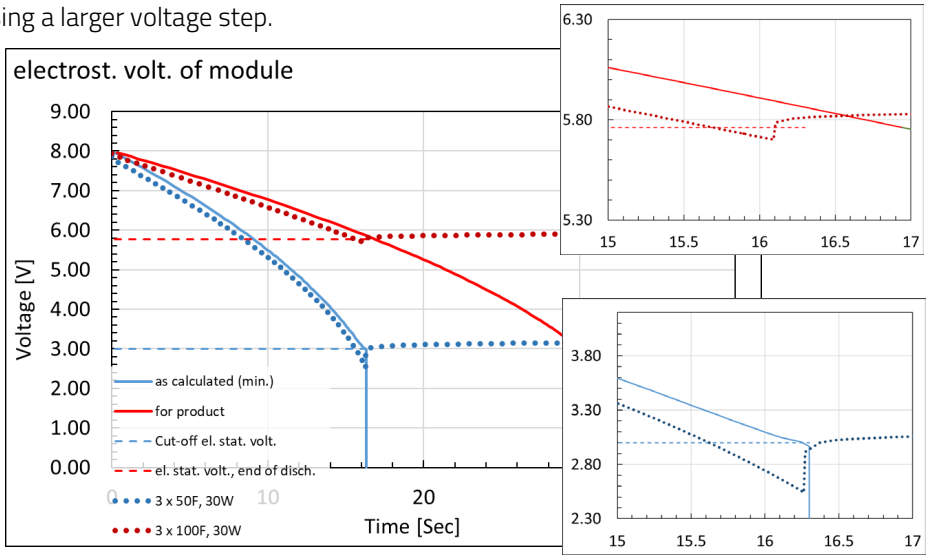


Figure 9: Calculated electrostatic voltage and measurement of dynamic discharge voltage. Insets show the voltage step caused by the ESR and the electrostatic voltage after discharge

Figure 10 shows that the calculation well describes measured graphs. Minor discrepancies stem from production tolerances, small contributions of the nonlinearity caused by the non-capacitive faradaic charge-storing process and the effect of the distributed network formed by the porous electrode of the EDLC. [3] [4] This leads to apparent variations of the device capacitance and, thus, a deviation from the calculation that assumes a constant capacitance throughout the discharge process. [5]

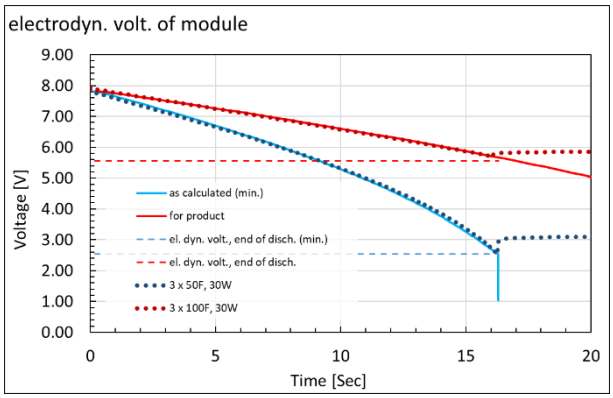


Figure 10: Calculated electrodynamic voltage and measurement of dynamic discharge voltage

Figure 11 shows a good agreement between measured and calculated current. As already mentioned above, slight deviations may arise from minor nonlinearities and production tolerances. The current for the 50 F stack is higher than for the 100 F stack to compensate for the lower voltage, i.e., faster voltage decrease over time, and thus, to ensure a constant 30 W output during the discharge.

The example given here suggests a generally good agreement between theory and measurement. Minor deviations can be explained by production tolerances and nonlinearities, which can be neglected for most practical applications.

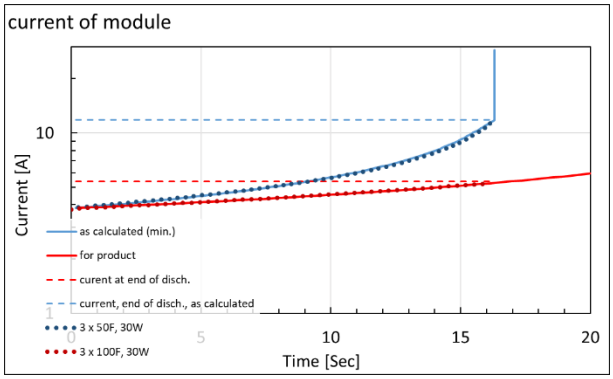


Figure 11: Calculated and measured current.

A APPENDIX

A.1 Literature

[1] G. Stana et al., Supercapacitor Constant-Current and Constant-Power Charging and Discharging Comparison under Equal Boundary Conditions for DC Microgrid Application, Energies, 6(10), 4167 (2023)

[2] H. Yang, Analysis of Supercapacitor Charge Redistribution through Constant Power Experiments, 2017 IEEE Power & Energy Society General Meeting, Chicago, IL, USA, pp. 1-5 (2017)

[3] Anis Allagui et al., Reevaluation of Performance of Electric Double-layer Capacitors from Constant-current Charge/Discharge and Cyclic Voltammetry, Scientific Reports, 6:38568 (2016)

[4] S. Fletcher et al., A universal equivalent circuit for carbon-based supercapacitors., J Solid State Electrochem, 18, 1377–1387 (2014)

[5] P. Mehra et al., A Comprehensive Analysis of Supercapacitors and Their Equivalent Circuits—A Review, World Electric Vehicle Journal, 15(8), 332 (2024)

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REVISION HISTORY

Document Version	Release Date	Changes
a	2025/06/11	Initial release of the application note
b	2026/11/09	Correction of **"Current at end of discharge"** page 4

Note: *The current version of the document and the release date are indicated in the footer of each page of this document.*